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H03F 1/32

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(56) Documents Cited
GB 2359466 A
GB 2337169 A
US 6141390 A
GB 2351624 A
WO 2001/008296 A1
US 5049832 A

(58) Field of Search
UK CL (Edition T) **H3W** WULCC WULCF WULPR
INT CL^7 **H03F** 1/32
Other: **Online: WPI, EPODOC, JAPIO**

(54) Abstract Title
An apparatus and method for power amplifier linearisation

(57) An input signal supplied to a modulator 18 for providing a first signal having a complex baseband vector, a second signal having a corrective vector selected from a look up table corresponding to the first complex baseband vector, a predistorter 20 for receiving said first and second signals and adding said first and second vectors together to provide a third signal having a desired predistortion vector for linearising the output signal of a power amplifier in the power amplifier system wherein the output signal has a amplification vector that is substantially equal to the complex baseband vector. The apparatus may be adapted to compensate I-Q imbalance in the down converter 25. An equaliser may be inserted after the predistorter to reduce linear memory effects.

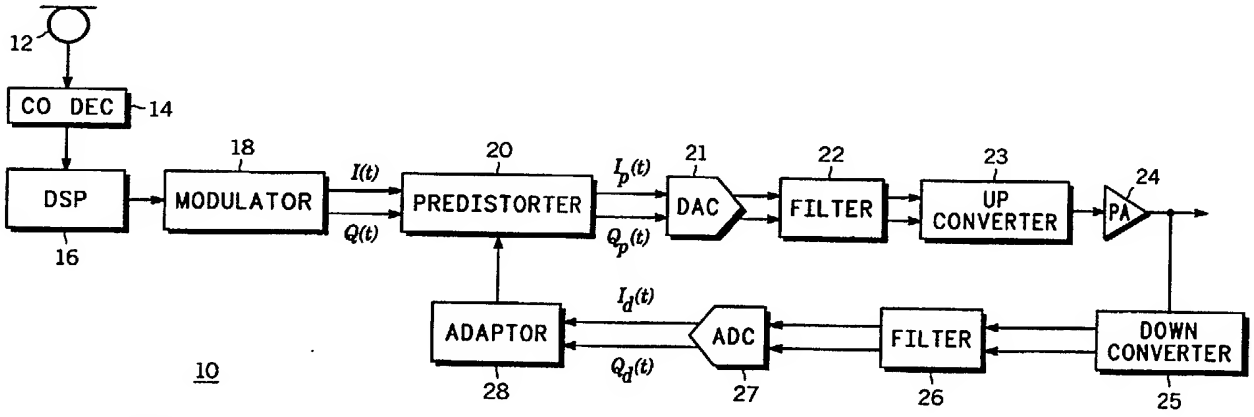

FIG. 1

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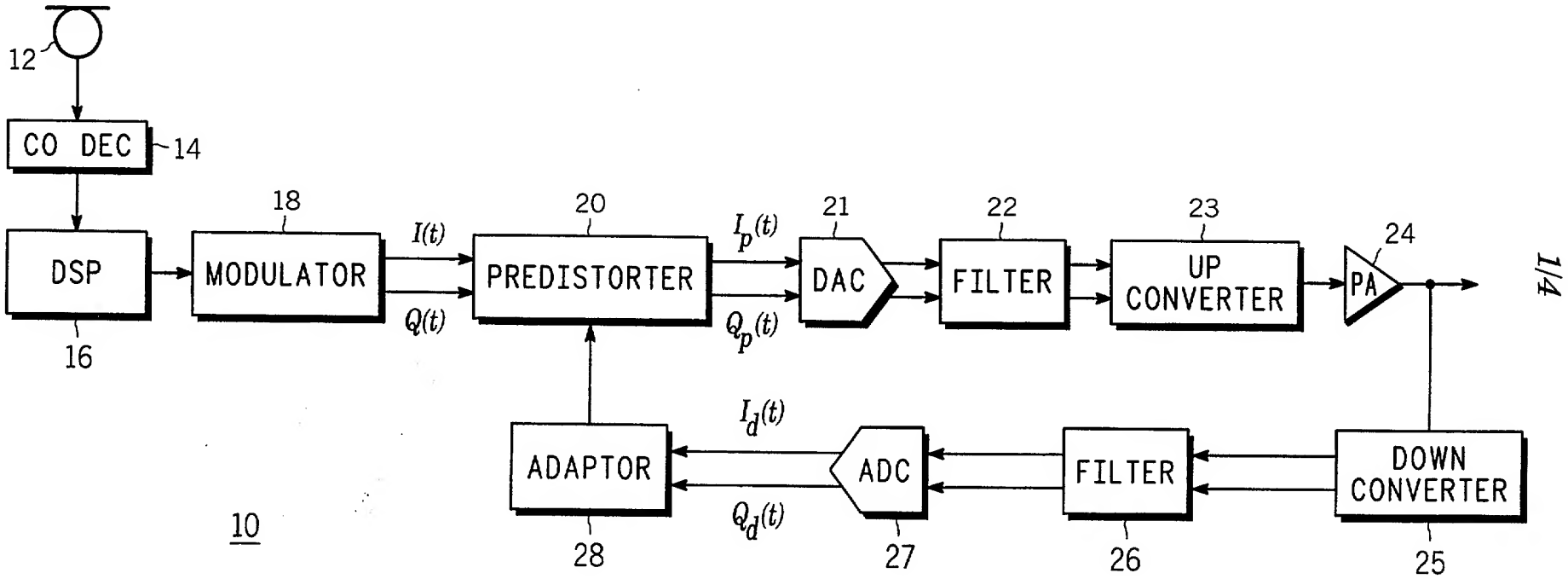

12
CO DEC
14
DSP
16
18
MODULATOR
I(t)
Q(t)
20
PREDISTORTER
$I_p(t)$
$Q_p(t)$
21
DAC
22
FILTER
23
UP CONVERTER
24
PA
ADAPTOR
28
$I_d(t)$
$Q_d(t)$
ADC
27
FILTER
26
DOWN CONVERTER
25
10

FIG. 1

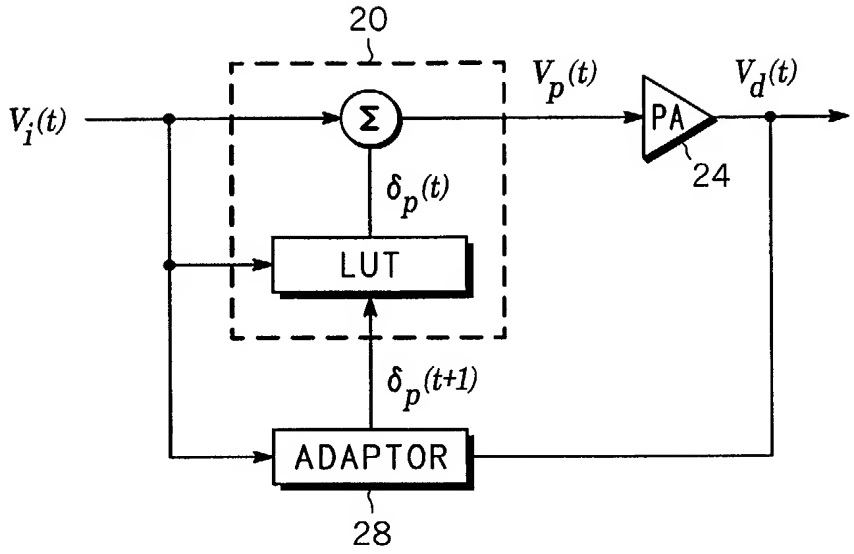


FIG. 2

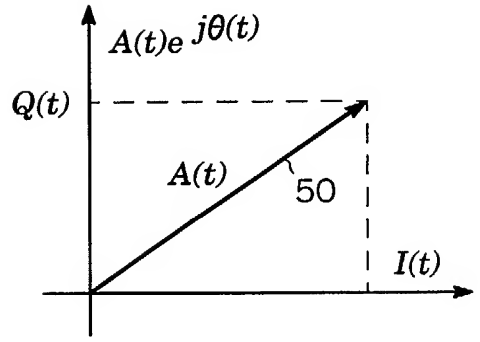


FIG. 3A

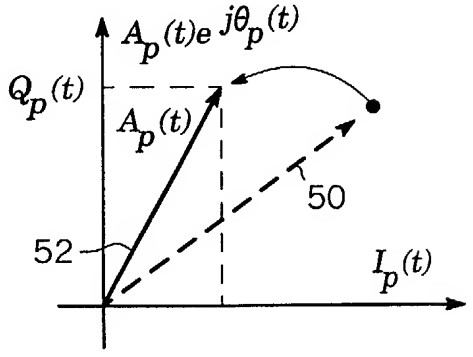


FIG. 3B

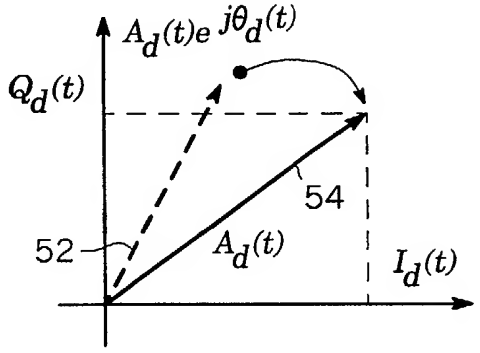


FIG. 3C

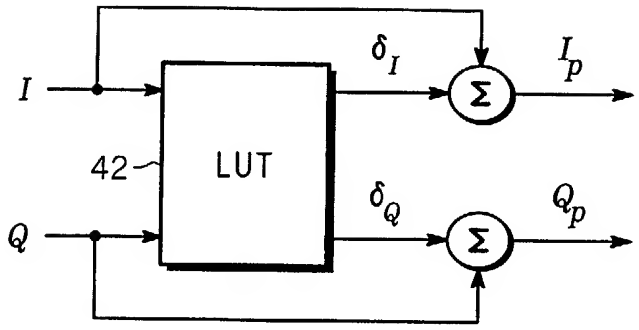
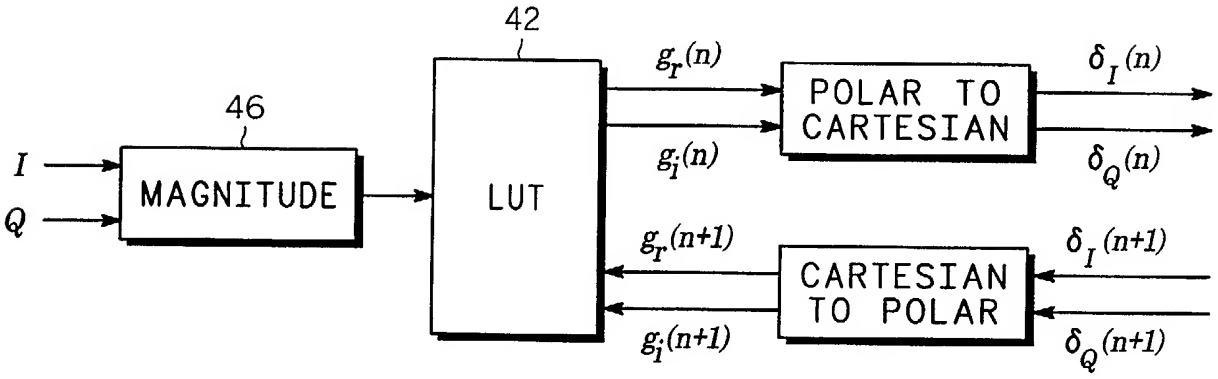

I
Q
42
LUT
δ_I
δ_Q
Σ
Σ
I_p
Q_p

FIG. 4

FIG. 5


I
Q
46
MAGNITUDE
42
LUT
$g_r(n)$
$g_i(n)$
POLAR TO CARTESIAN
$\delta_I(n)$
$\delta_Q(n)$
$g_r(n+1)$
$g_i(n+1)$
CARTESIAN TO POLAR
$\delta_I(n+1)$
$\delta_Q(n+1)$

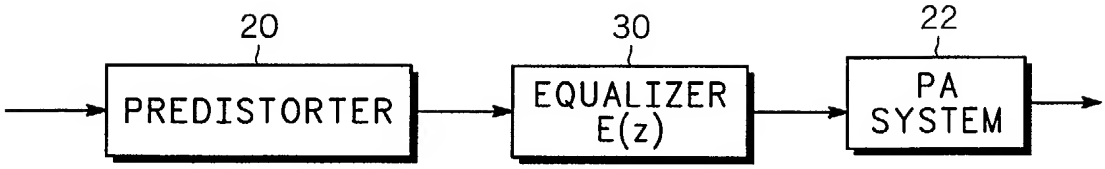
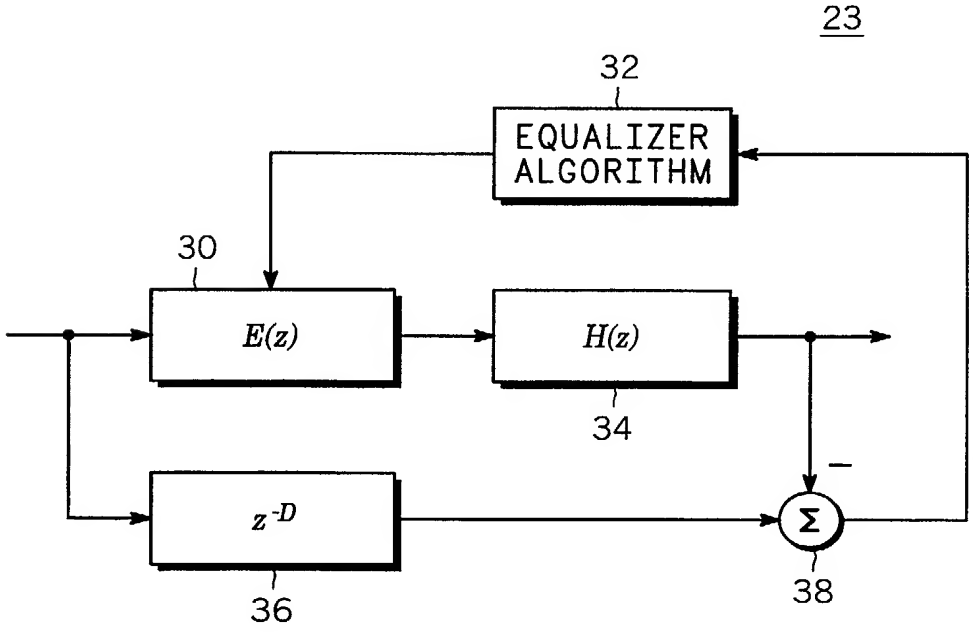

20
PREDISTORTER
30
EQUALIZER
E(z)
22
PA
SYSTEM

FIG. 6

FIG. 7


23
32
EQUALIZER
ALGORITHM
30
E(z)
H(z)
34
z -D
36
Σ
38
–

AN APPARATUS AND METHOD FOR POWER AMPLIFIER LINERISATION

FIELD OF THE INVENTION

The present invention relates generally to an apparatus and method for power amplifier linerisation. More specifically, the invention relates to a baseband digital predistorters for linerisation of non-linear power amplifiers.

BACKGROUND OF THE INVENTION

Linear power amplifiers are elements that are commonly used in both handsets and base-stations in mobile communication systems. Linear power amplifiers, although spectrally pure in the sense of generating spectral regrowth, are inherently power inefficient and hence costly in comparison to non-linear power amplifiers. In contrast, non-linear amplifiers are power efficient but spectrally impure. Linerisation of non-linear power amplifiers is employed to minimise the spectral impurities while capitalising on the inherent efficiency of non-linear power amplifiers.

Such transmitter schemes exist and are commonly used in mobile communication systems. For example, in next generation mobile communication equipment and systems, spectral efficiency, power efficiency, spectral purity, and cost implications are all critical factors taken into consideration to meet standards and specification requirements, and market demands. Thus, there is a need for a cost effective solution to the problem of linerisation of power efficient nonlinear power amplifiers.

US5049832 discloses amplifier linearization by adaptive predistortion by multiplicative or gain based

predistoration. However, such a proposal may be expensive, complex and difficult to realise in semiconductor circuitry, and may display unacceptable sensitivity to environmental hazards such as electronic noise.

Digital baseband predistortion methods like US5049832, may also suffer from memory effects. Such memory effects may be introduced, for example by virtue of reconstruction and anti-aliasing filters in systems employing such methods. These filters are required and are indispensable in for example protocols requiring wideband power amplifiers such as next generation (2.75G & 3G/UMTS) protocols. Memory effects if unchecked may be so severe to cause the system to fail system specifications.

In view of this, there is a need to provide an apparatus and method of linearisation of power efficient nonlinear power amplifiers that may be cost effectively realised in semiconductor circuitry, while providing acceptable sensitivity to electronic noise, to meet the increasingly stringent standards and specification requirements for advancing mobile communication systems.

STATEMENT OF THE INVENTION

In accordance with the invention there is provided an apparatus for power amplifier linearisation as claimed in claim 1, and a method for power amplifier linearisation as claimed in claim .

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be more fully described, by example, with reference to the drawings, of which:

FIG. 1 shows a block diagram of an apparatus and method for power amplifier linearisation according to an embodiment of the invention;

FIG. 2 shows a block diagram of an addition-based predistorter amplifier system in accordance with an embodiment of the invention;

FIG. 3A-3C shows a series of real/imaginary I-Q graphs for signals at various points in the system according to an embodiment of the invention;

FIG. 4 shows a block diagram of a look up table configuration in accordance with an embodiment of the invention;

FIG. 5 shows a block diagram of a look up table configuration in accordance with an embodiment of the invention;

FIG. 6 shows a block diagram of linearising memory based power amplifier nonlinearity system in accordance with an embodiment of the invention; and

FIG. 7 shows a block diagram of linearising memory based power amplifier nonlinearity system of FIG. 6 in greater detail in accordance with an embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

In linear modulation scheme applications, for example as used in next generation mobile communication systems and equipment, linearisation of non-linear power amplifiers is required. In FIG. 1, a block diagram of an apparatus and method for power amplifier linearisation according to an embodiment of the invention is shown. Specifically, an implementation of a power amplifier (PA) 24 with a baseband digital based adaptive predistorter 20 system comprises an encoder-decoder (CO DEC) 14 and

digital signal processor (DSP) 16 and a modulator 18 that provides a signal having components $\{I(t),Q(t)\}$ to adaptive baseband predistorter 20. The predistorter 20 may provide a signal to the non-linear power amplifier 24 via equaliser 21 (shown in FIGS. 6 and 7), which is discussed in further detail, digital-to-analogue converter (DAC) 21, reconstruction filter 22, and quadrature up converter 23 with input components $\{I_p(t),Q_p(t)\}$. The output 25 of amplifier is feedback to the predistorter 20 via down converter 25, antialiasing filter 26, (dual) analog-to-digital converter (ADC) 27, with signal with components $\{I_d(t),Q_d(t)\}$, and adaptor 28.

An embodiment of the predistorter 20 and adaptor 28 amplifier system is shown in greater detail in the block diagram of FIG. 2. The Look Up Table (LUT) is addressed by the amplitude of Vi(t) and has the contents of $\delta_p(t)$. Another element in the predistortor 20 is the adder Σ which adds $\delta_p(t)$ to the input Vi(t). Conventionally, power amplifier distortion is modelled as an amplitude-dependent complex gain. In the embodiment shown in FIGS. 1 and 2, with reference to FIGS. 3A-3C, the power amplifier is modelled as an amplitude-dependent additive offset. The predistortion is performed in predistorter 20 and adaptor 28 for each complex baseband vector that is the result of the digital modulation received from modulator 18. For each complex baseband vector, the predistorter 20 and adaptor 28 produce a corresponding corrective vector. The corrective vector is received from a look up table (LUT) 42 and added to the modulator vector to yield a desired predistortion vector, as shown in FIGS. 3A-3C. FIG. 3A is the "ideal" undistorter vector 50 supplied by the modulator 18 (as shown in FIG. 1). FIG. 3B is the predistorter vector 52 produced by

the predistorter. Fig. 3C is the distorted vector 54 resulting from the amplification stage sensed at 26 (as shown in FIG. 1). Preferably, after the application of the predistortion the vector resulting after the amplification stage 26 should be the same as the vector at the output of the modulator 18.

The circuit requirements may vary for different applications. One configuration includes two adders and the LUT 42 having addressing, for example, on the order of 2K words, and is shown in FIG. 4. Of course, this predistorter may be implemented digitally and be realised on either a DSP, FPGA or ASIC. The distortion incurred in the power amplifier 24 is amplitude or polar based, while the LUT 42 addressing is Cartesian. There are any number of Cartesian values {I,Q} that may produce the equivalent amplitude, $A^2 = I^2 + Q^2$. Accordingly, with this approach, there is some amount of redundancy. In order to maximise use of memory for the LUT, a ¼-wave symmetry compression may be applied to reduce memory requirements by approximately 75%.

In some applications that require less memory intensive techniques, for example mobile unit handsets in mobile communication systems, the size of the LUT 42 may be reduced, for example from 2K to 200 locations. One such technique is shown in FIG. 5, where the LUT 42 is structured in polar format. The LUT 42 in FIG. 5 is addressed by the amplitude and/or magnitude 46 instead of the I,Q pair, and the gain vector g_r, g_i instead of the corresponding addition vector δ_I, δ_Q is stored in the LUT 42. The corresponding gain vector is stored and converted to Cartesian format for employment in the subsequent predistortion stage. The adaptive or training stage of the predistorter then produces an improved

correction vector vector $\{\delta_I(n+1), \delta_Q(n+1)\}$, which is then converted back into polar format before being stored in the LUT 42 for subsequent re-employment. The conversions are realized by the following equations:

$$\delta_I(n) = (g_r(n)-1)I(n) - g_i(n)Q(n)$$
$$\delta_Q(n) = (g_r(n)-1)Q(n) - g_i(n)I(n) \quad \text{.....Polar to Cartesian}$$

$$g_r(n+1) = \frac{I(n)I_p(n) + Q(n)Q_p(n)}{\sqrt{I^2+Q^2}}$$
$$g_i(n+1) = \frac{I(n)Q_p(n) - Q(n)I_p(n)}{\sqrt{I^2+Q^2}} \quad \text{.....Cartesian to Polar}$$

It will be appreciated that the predistortion technique may be suited for compensation I/Q imbalance in quadrature down converters found in radio transceivers.

Power amplifier nonlinearity is commonly modelled as being memoryless and amplitude dependent, based on the assumption that the nonlinearity depends only on the current input amplitude and not on previous amplitudes. It has been shown in practice, however, that this assumption is incorrect. For instance, in baseband digital based predistorters, the reconstruction and antialising filters introduce a memory effect. Linearisation neutralises nonlinearity while equalisation neutralises frequency (or memory) base gain and phase distortion. FIG. 6 shows a block diagram of an example of linearising memory based power amplifier nonlinearity system shown for example in FIG. 1. In FIG. 7, which is FIG. 6 in greater detail, H(z) represents the linear memory effect of the filter 34 within the power amplifier system, E(z) is the equaliser 30, and D is the pure delay, corresponding to the combined group delay through the equaliser and filter. Referring to FIG. 1, the equaliser 30 is interposed between the predistorter 20

and the DAC-reconstruction filter and up converter 22. The technique first involves determining an inverse filter or equaliser for the filter dynamics in the loop by using a channel equaliser, which can be done for example in a predetermined manner, or using an adaptive approach if the filter dynamics vary. Then, the equaliser 30 is used to filter the predistorter outputs so that the combined dynamics of the equaliser 30 and the memory or filtering occurring in the power amplifier system reduce to that of a pure delay of D seconds. FIG. 6 illustrates the equaliser 30, which acts to buffer the power amplifier system, which includes filter 34 from the predistorter 20. The additive correction terms are updated according to the nonlinear iterative equation as:

$$\delta_I(t+1) = |\mu\varepsilon_I(t) - signI(t)\delta_I(t)|$$
$$\delta_Q(t+1) = |\mu\varepsilon_Q(t) - signQ(t)\delta_Q(t)| \quad \text{.....Original algorithm}$$

which is modified:

$$\delta_I(t+1-D) = |\mu\varepsilon_I(t-D) - signI(t-D)\delta_I(t-D)|$$
$$\delta_Q(t+1-D) = |\mu\varepsilon_Q(t-D) - signQ(t-D)\delta_Q(t-D)| \quad \text{.....Modified for delay of } D$$

Thus, an equaliser is used to reduce the filter dynamics within the power amplifier system to give a combined dynamic of a pure delay, and the training algorithm is modified to accommodate the effective delay within the loop. It will be appreciated that the specific configuration discussed in detail with reference to FIGS. 6 and 7, is one of many possible configurations to achieve the equalisation process.

It will be appreciated that although the particular embodiments of the invention have been described above, various other modifications and improvements may be made

by a person skilled in the art without departing from the scope of the present invention.

CLAIMS:

1. An apparatus for power amplifier linerisation for a power amplifier system comprising an input signal having an input amplitude supplied to a modulator for providing a first signal having a complex baseband vector, a second signal having a corrective vector selected from a look up table corresponding to the first complex baseband vector, a predistorter for receiving said first and second signals and adding said first and second vectors together to provide a third signal having a desired predistortion vector for linearising the output signal of a power amplifier in the power amplifier system wherein the output signal has a amplification vector that is substantially equal to the complex baseband vector.

2. An apparatus as claimed in claim 1 wherein the first signal complex baseband vector is an amplitude-dependent/polar based complex gain.

3. An apparatus as claimed in claim 1 or 2 wherein the second signal having a corrective vector is Cartesian based and the look up table addressing is Cartesian.

4. An apparatus as claimed in any preceding claim wherein the look up table addressing a ¼-wave symmetry compression is used.

5. An apparatus as claimed in claim 1 or 2 wherein look up table addressing is polar format.

6. An apparatus as claimed in claim 5 wherein the look up table addressing in polar format is converted to Cartesian format.

7. An apparatus as claimed in claim 6 wherein the look up table addressing in polar format is reconverted to Cartesian format.

8. An apparatus as claimed in any preceding claim wherein the apparatus is adapted for compensation I/Q imbalance in quadrature down converters.

9. An apparatus as claimed in any preceding claim further comprising an equaliser for minimise linear memory effects.

10. An apparatus as claimed in claim 9 wherein said equaliser is positioned between the predistorter and the output of the system.

11. An apparatus for power amplifier linerisation as substantially as hereinbefore described and with reference to the drawings.

12. A method for power amplifier linerisation for a power amplifier system comprising the steps of:

providing an input signal having an input amplitude supplied to a modulator for providing a first signal having a complex baseband vector;

providing a second signal having a corrective vector selected from a look up table corresponding to the first complex baseband vector;

receiving said first and second signals at a predistorter;

adding said first and second vectors together to provide a third signal having a desired predistortion vector for linearising the output signal of a power amplifier in the power amplifier system wherein the output signal has a amplification vector that is substantially equal to the complex baseband vector.

Application No: GB 0204047.5 **Examiner:** Brian Mc Cartan
Claims searched: 1 - 12 **Date of search:** 19 August 2002

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): H3W (WULPR, WULCF, WULCC)

Int Cl (Ed.7): H03F (1/32)

Other: ONLINE: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB 2359466 A	(NEC) See figure 1 and abstract	At least 1 & 12
X	GB 2351624 A	(Wireless) See figures 1 & 2 and abstract	At least 1 & 12
X	GB 2337169 A	(Nokia) See figure 1 (note 18, 58) and abstract	At least 1 & 12
X	WO 01/08296 A1	(Datum) See figures 1 - 3, abstract & page 2, line 5.	At least 1 & 12
X	US 6141390 A	(Cova) See figures 4 - 8 and col. 9, line 18 onwards	At least 1 & 12
X	US 5049832 A	(Cavers) Figure 5 and abstract	At least 1 & 12

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.